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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/603,219	06/24/2003	Anirban Rahut	X-1221 US	4298

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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 07/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/603,219	RAHUT ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on *24 June 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-11, 13-26, and 28-34* is/are rejected.

7)☒ Claim(s) *4,12 and 27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 06/24/2003. Claims 1- 34 are pending.

Claim Objections

The claims 31 and 33 are objected to because: the phrase "the computer automated tool " recited in the claims lacks of antecedent basis. Appropriate correction is required.

Drawings

The drawings are objected to because in Fig. 2, the referred element "path 2" is not specified in the specification. In the specification, it is referred to as "path 3".

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, and 5-6 are rejected under 35 U.S.C. 102(b) as being anticipated by Betz et al. (Betz) (US Patent No. 6763506).

Referring to claim 1, Betz discloses the method of estimating an upper-bound for an operational frequency of at least a portion of a placed circuit design comprising:

(a) identifying a clock source within the placed circuit design, wherein the clock source is associated with a clock domain (col. 12, lines 6-14);

(b) determining an initial routing of connections of the clock domain (Fig. 5, step 508; col. 11, lines 58+);

(c) determining a minimum path slack corresponding to each connection of the clock domain (Figure 5, step 512; col. 13, lines 24-59; Fig. 6B, step 655; col. 10, lines 32-34);

(d) selecting the connections based on minimum path slack (Fig. 6A, step 612; col. 12, lines 1-42); and

(e) routing one or more of the selected connections (col. 13, lines 60+) in delay mode (see abstract).

Referring to claim 5, Betz substantially discloses the method of claim 1, said step (c) further comprising:

assigning to each connection the path slack of the path within which the connection is disposed (Betz, col. 2, lines 21-26).

Referring to claim 6, Betz substantially discloses the method of claim 5, further comprising:

if more than one path passes through the connection, assigning to the connection the minimum path slack of all paths passing through the connection (Betz, col. 3, lines 15-30).

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. **Claim 7 is rejected** under 35 U.S.C. 103(a) as being unpatentable over Betz et al. (Betz) (US Patent No. 6763506) in view of Noll et al. (Noll) (US Patent No. 6058252).

Betz substantially discloses the method of claim 1, except the step (d) further comprising: populating a data structure with the connections of the clock domain; and sorting the connections according to the path slack of each connection.

Noll teaches a method and a system for generating effective layout constraints for a circuit design that use a data structure to organize and sort connection data in order of increasing slack (col. 33, lines 28-38; col. 34, lines 1-14, Fig. 15A and 15B).

Therefore, it would have been obvious to ordinary skill in the art to combine the method of Betz with the method disclosed by Noll because the combined method would provide more information about data structure to thereby enabling sorting connections based on path slack as required by routing tool and avoiding data duplication (col. 1, lines 57-63; col. 34, lines 11-16).

3. **Claims 2, 3, 8- 11, 13-26, and 28-34 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Betz et al. (Betz) (US Patent No. 6763506) in view of Bennett et al. (Bennett) (US Patent No. 5659484).

Referring to claim 2, Betz substantially discloses the method of claim 1, except the steps of: (f) marking the connections of the clock domain which have a lowest minimum path slack; and (g) identifying marked connections which are not routed in delay mode as selected.

Bennett teaches the path enumeration (corresponding to "marking") process (Bennett, col. 10, lines 48+; Fig. 2D; Fig. 5a) for the frequency driven layout design method comprising the steps of enumerating ("marking") the connections of the clock domain that have a lowest minimum path slack; and identifying marked connections which are not routed in delay mode as selected.

Therefore, it would have been obvious to ordinary skill in the art to combine the method of Betz with the method disclosed by Bennett because the combined method would provide an efficient designed timing analysis techniques to analyze and identify circuit paths and associated maximum delays need to operate at a target frequency (Bennett, col.5, 61-64).

Referring to claim 3, the method of claim 2, wherein the connections having the lowest minimum path slack correspond to a critical path, said method further comprising:

(h) determining an upper-bound estimate of clock frequency for said clock domain as defined by a path delay of the critical path (Betz , col. 12, lines 47-50).

Referring to claim 8, the method of claim 3, further comprising:

iteratively applying steps (a) - (h) to different clock sources of the placed circuit design, wherein each different clock source is associated with a corresponding and different clock domain (Fig. 5, step 520).

Referring to claims 9, 10, 17, 24, 25, and 33, Betz teaches the method, within a computer automated tool (system/computer readable storage stored computer program codes), of estimating an upper-bound of an operational frequency of at least a portion of a placed circuit design comprising:

(a) constraining at least two clock sources within the placed circuit design to a same target frequency (Betz, col. 12, lines 6-14), wherein each clock source is associated with a different clock domain;

(b) determining an initial routing of connections of the clock domains (Fig. 5, step 508; col. 11, lines 58+);

(c) determining a minimum path slack corresponding to each connection of the plurality of clock domains (Figure 5, step 512; col. 13, lines 24-59; Fig. 6, step 655; col. 10, lines 32-34);

Thus, Betz substantially teaches all the elements in claims 9, 24, and 33 except the steps of:

(d) marking connections of the plurality of clock domains which have a lowest minimum path slack;

(e) identifying marked connections which are not routed in delay mode; and
(f) routing one or more of the identified connections in delay mode .
(g) repeating steps (c) - (f) until all marked connections are routed in delay mode.

Bennett teaches the path enumeration (corresponding to "marking") process (Bennett, col. 10, lines 48+; Fig. 2D; Fig. 5a) for the frequency driven layout design method comprising the steps of enumerating ("marking") the connections of the plurality of clock domain that have a lowest minimum path slack; identifying marked connections which are not routed in delay mode; routing one or more of the identified connections in delay mode; and the repetitive step to complete the routing process (Fig. 5a, Fig. 5b, Fig. 6a, Fig. 6b, and Fig. 6c).

Therefore, it would have been obvious to ordinary skill in the art to combine the method of Betz with the method disclosed by Bennett because the combined method would allow routing tool able to identify connections to be processed.

Referring to claims 16 and 31, Betz teaches the machine-readable storage (the computer automated tool/ system), having stored thereon a computer program having a plurality of code sections executable by a machine (col. 19, lines 42-62) for causing the machine to perform the steps of:
(a) identifying a clock source within a placed circuit
design, wherein the clock source is associated with a clock
domain (col. 12, lines 6-14);
(b) determining an initial routing of connections of
the clock domain (Fig. 5, step 508; col. 11, lines 58+);
(c) determining a minimum path slack corresponding to
each connection of the clock domain (Figure 5, step 512; col. 13, lines 24-59; Fig. 6B, step 655; col. 10, lines 32-34);

Thus, Betz substantially teaches all the elements in claims 16 and 31 except the steps of:
(d) marking connections of the clock domain which have
a lowest minimum path slack;

(e) identifying marked connections which are not routed
in delay mode; and
(f) routing one or more of the identified connections
in delay mode.

Bennett teaches the path enumeration (corresponding to "marking") process (Bennett, col. 10, lines 48+; Fig. 2D; Fig. 5a) for the frequency driven layout design method comprising the steps of enumerating ("marking") the connections of the plurality of clock domain that have a lowest minimum path slack; identifying marked connections which are not routed in delay mode; routing one or more of the identified connections in delay mode; and the repetitive step to complete the routing process (Fig. 5a, Fig. 5b, Fig. 6a, Fig. 6b, and Fig. 6c).

Therefore, it would have been obvious to ordinary skill in the art to combine the method of Betz with the method disclosed by Bennett because the combined method would provide an efficient designed timing analysis technique to analyze and identify circuit paths and associated maximum delays need to operate at a target frequency (Bennett, col.5, 61-64).

Referring to claim 11, the method of claim 10, wherein the connections having the lowest minimum path slack correspond to a critical path, said method further comprising:

determining an upper-bound estimate of clock frequency for the clock domains as defined by a path delay of the critical path (Betz , col. 12, lines 47-50).

Referring to claim 13, the method of claim 10, said step (c) further comprising:

assigning to each connection the path slack of the path within which the connection is disposed (Betz, col. 2, lines 21-26).

Referring to claim 14, the method of claim 13, further comprising:

if more than one path passes through the connection, assigning to the connection the minimum path slack of all paths passing through the connection (Betz, col. 3, lines 15-30).

Referring to claim 18, the machine readable storage of claim 17, wherein the connections having the lowest minimum path slack correspond to a critical path, said machine readable storage further causing the machine to perform the step of:

(h) determining an upper-bound estimate of clock frequency for said clock domain as defined by a path delay of the critical path (Betz , col. 12, lines 47-50).

Referring to claim 19, the machine readable storage of claim 16, wherein the initial routing is performed in a resource mode (Bennett, col. 33, lines 21-23).

Referring to claim 20, the machine readable storage of claim 16, said step (c) further comprising:

assigning to each connection the path slack of the path within which the connection is disposed (Betz, col. 2, lines 21-26).

Referring to claim 21, the machine readable storage of claim 20, further comprising:

if more than one path passes through the connection, assigning to the connection the minimum path slack of all paths passing through the connection (Betz, col. 3, lines 15-30).

Referring to claim 23, the machine readable storage of claim 18, further comprising:

iteratively applying steps (a)-(h) to different clock sources of the placed circuit design, wherein each different clock source is associated with a corresponding and different clock domain (Betz, Fig. 5, step 520).

Referring to claim 26, the machine readable storage of claim 25, wherein the connections having the lowest minimum path slack correspond to a critical path, said machine readable storage further causing the machine to perform the step of:

determining an upper-bound estimate of clock frequency for the clock domains as defined by a path delay of the critical path (Betz , col. 12, lines 47-50).

Referring to claim 28, the machine readable storage of claim further comprising:

assigning to each connection the path within which the connection is disposed (Betz, col. 2, lines 21-26)

Referring to claim 29, the machine readable storage of claim 28, further comprising:

if more than one path passes through the connection, assigning to the connection the minimum path slack of all paths passing through the connection (Betz, col. 3, lines 15-30).

Referring to claim 32, the system of claim 31, wherein the connections having the lowest minimum path slack correspond to a critical path,
said system further comprising:

means for determining an upper-bound estimate of clock frequency for the clock domain as defined by a path delay of the critical path (Betz , col. 12, lines 47-50).

Referring to claim 34, the system of claim 33, wherein the connections having the lowest minimum path slack correspond to a critical path, said system further comprising:

means for determining an upper-bound estimate of clock frequency for the clock domains as defined by a path delay of the critical path (Betz , col. 12, lines 47-50).

4. **Claims 15, 22, and 30 are rejected** under 35 U.S.C. 103(a) as being unpatentable over Betz et al. (Betz) (US Patent No. 6763506) in view of Bennett et al. (Bennett) (US Patent No. 5659484), and in further view of Noll et al. (Noll) (US Patent No. 6058252).

Betz and Bennett substantially disclose all limitations in the claims except the steps comprising: populating a data structure with the connections of the clock domain; and sorting the connections according to the path slack of each connection.

Noll teaches a method and a system for generating effective layout constraints for a circuit design that use a data structure to organize and sort connection data in order of increasing slack (col. 33, lines 28-38; col. 34, lines 1-14).

Therefore, it would have been obvious to ordinary skill in the art to combine the method of Betz with the method disclosed by Noll because the combined method would provide an efficient way for manipulating data (col. 1, lines 57-63; col. 34, lines 11-14).

Allowable Subject Matter

Claims 4, 12, and 27 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The prior art of record does not teach or fairly suggest, wherein the initial routing is performed in an overlap tolerant resource mode.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-293-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
Patent Examiner
Art Unit 2825

VUTHE SIEK
PRIMARY EXAMINER